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Dated: April 2, 2004 Signature: Valerie Cohen
(Valerie Cohen)

Docket No.: 388682000400
(PATENT)

4/8/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:
Ranjit J. ROZARIO et al.

Application No.: 09/740,669 Art Unit: 2182

Filed: December 18, 2000 Examiner: J. Schneider

For: SCHEDULER FOR A DATA MEMORY ACCESS HAVING MULTIPLE CHANNELS

BRIEF ON APPEAL

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on February 2, 2004. In accordance with 37 C.F.R. § 1.192, this Brief, along with the Appendix, is filed in triplicate and is accompanied by the required fee.

sf-1675851

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P § 1206:

I. Real Party in Interest
II. Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Invention
VI. Issues
VII. Grouping of Claims
VIII. Arguments
IX. Claims Involved in the Appeal
Appendix A. Claims

I. Real Party in Interest

The real party in interest for this appeal is:

Redback Networks, Inc., a Delaware corporation, with a principal place of business in San Jose, California.

II. Related Appeals and Interferences

There are no known related appeals or interferences, which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. Status of Claims

Claims 1-24 are pending in the present application. Claims 1-5, 9-14 and 19-24 are rejected. Claims 6-8 and 15-18 are objected to.

IV. Status of Amendments

No amendments to the application were submitted after final rejection.

V. Summary of Invention

The claimed inventions are directed to scheduling multiple channels. For example, claim 1 is directed to an apparatus to schedule a Direct Memory Access (DMA) device having multiple channels. (See page 9, lines 5-8 and 16-21, and Figs. 3 and 4.) The apparatus of claim 1 includes a shift structure with entries corresponding to the multiple channels to be schedule. (See page 12, lines 14-17, and Fig. 6.) Each entry in the shift structure includes a plurality of fields and a weight determined based on the fields. (See page 13, line 6, Fig. 6, page 15, lines 9 and 10.) The apparatus of claim 1 also includes a comparison-logic circuit configured to sort the entries of the shift structure based on their respective weights. (See page 15, lines 8 and 9, page 16, lines 3 and 4.)

VI. Issues

A. Whether claims 5-8 and 14-18 contain subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention under 35 U.S.C. 112, first paragraph.

B. Whether the invention disclosed in claim 9 is inoperative and therefore lacks utility under 35 U.S.C. 101.

C. Whether claims 1-4, 10-13 and 19-24 are unpatentable over U.S. Patent No. 5,504,919 (the Lee reference) in view of U.S. Patent No. 6,052,375 (the Bass reference) under 35 U.S.C. 103(a).

VII. Grouping of Claims

For purposes of this appeal brief only, and without conceding the teachings of any prior art references, the claims have been grouped as indicated below:

Claims 5-8 and 14-18 stand or fall together. Claim 9 stands alone. Claims 1-4, 10-13, and 19-24 stand or fall together.

VIII. Arguments

In an Office Action mailed on May 9, 2003 (Paper No. 6), the Examiner rejected claims 5-8 and 14-18 under 35 U.S.C. 112, first paragraph, claim 9 under 35 U.S.C. 101, and claims 1-4, 10-13 and 19-24 under 35 U.S.C. 103(a). In response, Applicants filed an Amendment on August 11, 2003. In a Final Office Action mailed on October 2, 2003 (Paper No. 6), the Examiner maintained the rejection of claims 5-8 and 14-18 under 35 U.S.C. 112, first paragraph, claim 9 under 35 U.S.C. 101, and claims 1-4, 10-13 and 19-24 under 35 U.S.C. 103(a). Applicants respectfully requests reversal of the rejection of these claims in view of the following remarks.

A. Rejection of claims 5-8 and 14-18 under 35 U.S.C. 112, first paragraph

As noted above, in the Final Office Action, the Examiner maintained the rejection of claims 5-8 and 14-18 under 35 U.S.C. 112, first paragraph. In particular, the Examiner rejected claims 5 and 14 on the ground that the term "in-flight" is not established in the art, and does not enable one skilled in the art to practice or understand the invention. The Examiner stated, "[i]t remains unclear how a packet can be both being processed and waiting to be scheduled for DMA transfer, so that it would be usable with the invention." The Examiner further stated, "[i]t would instead seem that as set forth by the specification, the field would indicate that the data transfer is already in progress, and there is not in need of being schedule."

Applicants assert that the notion that a packet can be in-flight and yet be scheduled in the DMA is consistent, particularly in view of the present specification. In particular, page 14, lines 20-22 of the present specification states, "a packet is considered to be in-flight when the packet is being processed, such as if a packet is being read out of memory, being sent out onto the bus, and the like."

Note that one of the examples provided in the present specification of an in-flight packet is a packet that is being sent out onto a bus. Also note that page 4, lines 17-21 of the present specification describes and Fig. 2 depicts a DMA that is a component of a packet processor ASIC (PPA). Page 3, lines 13-21 of the present specification describes and Fig. 1 depicts a PPA that is a component of a line card. In particular, page 3, lines 16 and 17 states that a backplane interface, which is another component of a line card, "can be configured to connect to any number of additional line cards on a mesh, a common bus, and the like."

Thus, when the DMA is a component of a line card connected to a bus, an in-flight packet can be a packet that is being sent out on the bus by the line card. However, before the in-flight packet is sent out on the bus, the in-flight packet can be first scheduled in the DMA on the line card.

Therefore, Applicants assert that claims 5 and 14, and claims 6-8 and 15-18 that depend from claims 5 and 14, are enabled.

B. Rejection of claim 9 under 35 U.S.C. 101

In the Final Office Action, the Examiner maintained the rejection of claim 9 under 35 U.S.C. 101 as being inoperative and therefore lacking utility. In particular, the Examiner asserted that the shift structure, which is recited in claim 1, could not be embodied as a FIFO device. The Examiner stated that: "A FIFO device by definition is processed in a very linear fashion. The first object added is the first object removed, not allowing for shifting, or sorting."

Applicants assert that the apparatus recited in claims 1 and 9 are operable. In particular, claim 1 recites a shift structure having a plurality of entries. Claim 1 also recites a comparison-logic circuit configured to sort the entries. Claim 9 recites that the shifting structure is a FIFO device. Thus, the apparatus recited by claim 9 is:

> a FIFO device having a plurality of entries corresponding to the multiple channels to be scheduled, wherein each entry in said shift structure includes a

plurality of fields, and wherein each entry includes a weight that is determined based on said plurality of fields; and

a comparison-logic circuit configured to sort said entries based on their respective weights.

Note that in the apparatus recited by claim 9, it is the comparison-logic circuit that sorts the entries of the FIFO device. Claim 9 recites an apparatus having a comparison-logic circuit configured to sort entries of a FIFO device rather than a process.

Therefore, Applicants assert that the apparatus recited in claim 9 has utility under 35 U.S.C. 101.

C. Rejection of claims 1-4, 10-13 and 19-24 under 35 U.S.C. 103(a)

In the Final Office Action, the Examiner maintained the rejection of claim 1-4, 10-13 and 19-24 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,504,919 (the Lee reference) in view of U.S. Patent No. 6,052,375 (the Bass reference).

The Examiner conceded that the Lee reference does not disclose entries having a plurality of fields. The Examiner asserted that the Bass reference teaches a plurality of fields in a parameter table, and that queues are sorted for output to a traffic queue allocation manager. In the Final Office Action, the Examiner stated, "Bass teaches a plurality of fields used in the arbitration of packets in a DMA scheduler."

While the Bass reference may disclose fields in a parameter table, independent claims 1, 10 and 19 recite that **each entry in a shift structure** includes a plurality of fields. In particular, claim 1 recites, in part, "each entry in said shift structure includes a plurality of fields." Claim 10 recites, in part, "writing a plurality of entries in a shift structure, wherein each entry is associated with a channel on the DMA, and wherein each entry includes a plurality of fields." Claim 19 recites, in

part, "assigning weights to a plurality of entries in a shift structure, wherein each entry is associated with a channel, and wherein each entry includes a plurality of fields."

In contrast, as depicted in FIGS. 1 and 9 of the Bass reference, the parameters in TSPT 7 are not fields in an entry of queues Q0 – Q31. Moreover, as depicted in FIG. 8, the parameters contained in TSPT 7 relate to the queues and not to the entries in the queues.

Thus, Applicants assert that the combination of the Lee reference and the Bass reference fails to teach or suggest all of the claim limitations of independent claims 1, 10 and 19. Thus, Applicants assert that claims 1, 10 and 19 are patentable over the combination of the Lee reference and the Bass reference. Additionally, Applicants assert that dependent claims 2-4, 11-13 and 20-24 are patentable for at the least reason that they depend from allowable independent claims.

IX. Claims Involved in the Appeal

A copy of the claims involved in the present appeal is attached as Appendix A. The claims in Appendix A include the amendments filed by Applicant on August 11, 2003.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 388682000400. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: April 2, 2004

Respectfully submitted,

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Attached: Appendix A (copy of claims involved in the appeal)

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Appendix A

Claim 1 (Previously Presented): An apparatus for scheduling a Direct Memory Access (DMA) device having multiple channels, comprising:

a shift structure having a plurality of entries corresponding to the multiple channels to be scheduled, wherein each entry in said shift structure includes a plurality of fields, and wherein each entry includes a weight that is determined based on said plurality of fields; and

a comparison-logic circuit configured to sort said entries based on their respective weights.

Claim 2 (Original): The apparatus of claim 1, wherein said comparison-logic circuit is configured to compare the weight of an entry being written into said shift structure with the weight of said entries in said shift structure.

Claim 3 (Original): The apparatus of claim 2, wherein said comparison-logic circuit is configured to insert said entry being written into said shift structure behind entries with higher weights and to shift entries with lower weights behind said entry being written into said shift structure.

Claim 4 (Original): The apparatus of claim 1, wherein said weight includes a number having a plurality of bits, and wherein each of said plurality of fields are assigned to a set of bits of said weight.

Claim 5 (Original): The apparatus of claim 4, wherein said plurality of fields includes:

an enable field, wherein said enable field is assigned to the-most-significant bit of said weight;

an output-ready field, wherein said output-ready field is assigned to the second-most-significant bit of said weight;

an input-ready field, wherein said input-ready field is assigned to the third-most-significant bit of said weight;

an in-flight field, wherein said in-flight field is assigned to the fourth-most significant bit of said weight; and

a priority field, wherein said priority field is assigned to the fifth-most significant bit to the tenth-most significant bit of said weight.

Claim 6 (Original): The apparatus of claim 5, wherein said priority field includes a plurality of priority levels, and wherein higher priority levels are assigned higher weights.

Claim 7 (Original): The apparatus of claim 6, wherein the channels of the DMA are connected to a synchronized optical network (SONET) having a plurality of optical carrier (OC) numbers, and wherein said plurality of entries are assigned priority levels corresponding to the OC numbers of the channels associated with said plurality of entries.

Claim 8 (Original): The apparatus of claim 7, wherein:

a first set of entries associated with channels operating at OC 12 are assigned a priority level of 12; and

a second set of entries associated with channels operating at OC 3 are assigned a priority level of 3.

Claim 9 (Original): The apparatus of claim 1, wherein said shifting structure is a First-In-First-Out (FIFO) device.

Claim 10 (Previously Presented): A method of scheduling multiple channels on a Direct Memory Access (DMA) device, comprising:

writing a plurality of entries in a shift structure, wherein each entry is associated with a channel on the DMA, and wherein each entry includes a plurality of fields;

assigning weights to said entries based on said plurality of fields;

sorting said entries based on said weights, wherein an entry having the highest weight is sorted to the head of said shift structure; and

reading said entry from the head of said shift structure to service the channel associated with said entry.

Claim 11 (Original): The method of claim 10 further comprising the step of:

writing said entry read from the head of said shift structure back into said shift structure after the channel associated with said entry is serviced.

Claim 12 (Original): The method of claim 11, wherein said writing step further comprises:

inserting said entry back into said shift structure behind entries in said shift structure with higher weights; and

shifting said entries in said shift structure with lower weights behind said entry to be written back.

Claim 13 (Original): The method of claim 10, wherein said weight includes a number having a plurality of bits, and said assigning step further comprises:

assigning each of said plurality of fields to a set of bits of said weight.

Claim 14 (Original): The method of claim 13, wherein said plurality of fields includes:

an enable field, wherein said enable field is assigned to the-most-significant bit of said weight;

an output-ready field, wherein said output-ready field is assigned to the second-most-significant bit of said weight;

an input-ready field, wherein said input-ready field is assigned to the third-most-significant bit of said weight;

an in-flight field, wherein said in-flight field is assigned to the fourth-most significant bit of said weight; and

a priority field, wherein said priority field is assigned to the fifth-most significant bit to the tenth-most significant bit of said weight.

Claim 15 (Original): The method of claim 14 further comprising the step of:

enabling said input-ready field of an entry when the channel associated with said entry is to be serviced.

Claim 16 (Original): The method of claim 14, wherein said priority field includes a plurality of priority levels, and further comprising the step of:

assigning higher weights to higher priority levels.

Claim 17 (Original): The method of claim 16, wherein the channels are connected to a synchronized optical network (SONET) having a plurality of optical carrier (OC) numbers, and further comprising the step of:

assigning priority levels corresponding to the OC numbers of the channels.

Claim 18 (Original): The method of claim 17 further comprising the steps of:

assigning a priority level of 12 to a first set of entries associated with channels operating at OC 12; and

assigning a priority level of 3 to a second set of entries associated with channels operating at OC 3.

Claim 19 (Original): A method of scheduling multiple channels, said method comprising:

assigning weights to a plurality of entries in a shift structure, wherein each entry is associated with a channel, and wherein each entry includes a plurality of fields;

sorting said entries based on said weights, wherein an entry having the highest weight is sorted to the head of said shift structure;

reading said entry from the head of said shift structure;

servicing the channel associated with said entry read from said shift structure; and

writing said entry read from said shift structure back into said shift structure.

Claim 20 (Original): The method of claim 19, wherein said writing step further comprises:

inserting said entry back into said shift structure behind entries in said shift structure with higher weights; and

shifting said entries in said shift structure with lower weights behind said entry to be written back.

Claim 21 (Original): The method of claim 19, wherein said weight includes a number having a plurality of bits, and said assigning step comprises:

assigning each of said plurality of fields to a set of bits of said weight.

Claim 22 (Original): The method of claim 19, wherein said plurality of fields includes a priority field having a plurality of priority levels.

Claim 23 (Original): The method of claim 22, wherein the channels are connected to a synchronized optical network (SONET) having a plurality of optical carrier (OC) numbers, and further comprising the step of:

assigning priority levels corresponding to the OC numbers of the channels.

Claim 24 (Original): The method of claim 23 further comprising the steps of:

assigning a priority level of 12 to a first set of entries associated with channels operating at OC 12; and

assigning a priority level of 3 to a second set of entries associated with channels operating at OC 3.